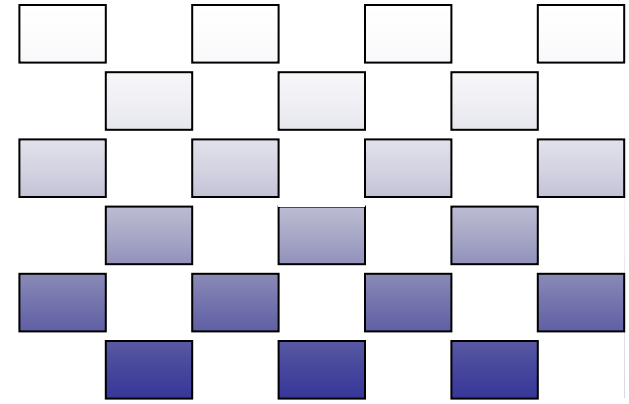

"ALWAYS COMPLETE"

Cogent CSB1726
Marvell MV78x60
System On a Module (SOM)

Hardware Reference Manual

Cogent Computer Systems, Inc.

Table of Contents

1 Warranty 4
2 Operating Specifications 5
2.1 CSB1726 Operating specifications 5
3 Overview 6
3.1 Introduction 6
3.2 Block Diagram 6
4 On-Board Devices 8
4.1 CSB1726 Address Map 8
4.2 2Gbyte DDR3-1066 SDRAM 8
4.3 512MByte 8-Bit NAND Flash 8
4.3.1 NAND Flash Notes 9
4.4 8MByte SPI NOR Flash 9
4.4.1 SPI NOR Flash Notes 10
4.5 24AA00T EEPROM 10
4.6 Marvell 88E1322 Dual PHY 10
4.6.1 88E1322 Interface Notes 11
4.7 ATXMEGA16A4 IPM Microcontroller 11
5 MV78x60 On-Chip Peripherals 12
5.1 Overview 12
5.2 MV78x60 to MXM Peripheral Mapping 12
5.3 MV78x60 Chip Selects 13
5.4 MV78x60 Multi- Purpose Pin Assignments 13
5.5 MV78x60 UARTS 15
5.6 MV78x60 I2C Interfaces 15
5.7 MV78x60 Local Bus Interface 16
5.8 MV78x60 High Speed SERDES PORTS 16
5.8.1 MV78x60 High Speed SERDES Notes 17
5.9 MV78x60 USB Controller 17
5.10 MV78x60 LCD Controller 17
6 CSB1726 Clocking 18
6.1 MV78x60 Input Clocks 18
6.2 MV78x60 Output Clocks 18
6.3 88E1322 Clock 18
7 CSB1726 Power Management 19
7.1 Overview 19
7.2 ATXMEGA16A4 IPM Microcontroller 19
7.2.1 ATXMEGA16A4 Microcontroller Notes 20
7.3 IPM Configuration Interface 21
7.3.1 IPM Configuration Interface Notes 21
7.4 IPM Power Supply Interface 21
7.4.1 IPM Power SUpply Interface Notes 22
8 MV78x60 Configuration 23
8.1 Overview 23
8.2 Default Configuration 23
9 CSB1726 Software 25
9.1 Overview 25
10 MXM Format/Pinout 26
10.1 Overview 26
10.2 MXM Format 26
10.3 MXM Connector 28
10.3.1 MXM Connector Notes 29
10.4 MXM Connector Pinouts 29
11 Document Revisions 39

List of Tables

Table 1 – CSB1726 Operating Specifications 5
Table 2 – CSB1726 Address Map 8
Table 3 – MV78x60 to NAND Flash Connections 9
Table 4 – MV78x60 to SPI NOR Flash Connections 9
Table 5 – MV78x60 to 24AA00T EEPROM Connections 10
Table 6 – MV78x60 to 88E1322 Connections 11
Table 7 – MV78x60 to MXM Port Mapping 13
Table 8 – MV78x60 MPP Pin Assignments 15
Table 9 – MV78x60 to MXM UART Connections 15
Table 10 – MV78x60 to MXM I2C Connections 16
Table 11 – MV78x60 SERDES to MXM Port Mapping 16

Table 12 – MV78x60 Input Clocks 18
Table 13 – MV78x60 Output Clocks 18
Table 14 – ATXMEGA16A4 Peripheral and GPIO usage 20
Table 15 – IPM Configuration Interface Bit Assignments 21
Table 16 – IPM Power Supply Interface Bit Assignments 22
Table 17 – MV78x60 Configuration Settings 24
Table 18 – CSB1726 Connector to Mated Height 29
Table 19 – CSB1726 MXM Connector Pinout 38
Table 20 – Document Revisions 39

List of Figures

Figure 1 – CSB1726 Block Diagram 7
Figure 2 – CSB1726 Top Side Placement 27
Figure 3 – CSB1726 Bottom Side Placement 28

1 WARRANTY

The enclosed product ("the Product"), a part of the Cogent Single Board series, is warranted by Cogent Computer Systems, Inc. ("Cogent") for a period of one year for reasonable development, testing and use, all as further described and defined below. This warranty runs solely to the individual or entity purchasing the Product and is not transferable or assignable in any respect. This warranty is valid only for so long as the product is used intact as shipped from Cogent. Any attempt or effort to alter the Product, including but not limited to any attempt to solder, de-solder, unplug, replace, add or affix any part or component of or onto the Product, other than components specifically intended for the user to plug and unplug into appropriate sockets and/or connectors to facilitate user programming, development and deployment, all as specifically described and authorized in this Product Hardware Reference Manual, shall void this warranty in all respects. Coverage under this warranty requires that the Product be used and stored at all times in conditions with proper electrostatic protection necessary and appropriate for a complex electronic device. These conditions include proper temperature, humidity, radiation, atmosphere and voltage (standard commercial environment, 0C to +70C, <60%RH). Any Product that has been modified without the express, prior written consent of Cogent is not covered by this warranty. The use or connection of any test or bus connector, adapter or component with any device other than a Cogent connector or adapter shall void this warranty and the warranty of all other components, parts and modules connected to the rest of the system. Cogent shall not be responsible for any damage to the Product as a result of a customer's use or application of circuitry not developed or approved by Cogent for use on or in connection with the Product.

This warranty does not cover defects caused by electrical or temperature fluctuations or from stress resulting from or caused by abuse, misuse or misapplication of the Product. Any evidence of tampering with the serial number on the Product shall immediately void this warranty. This Product is not intended to be used on or embedded in or otherwise used in connection with any life sustaining or life saving product and this warranty is not applicable nor is Cogent liable in any respect if the Product is so used. Notwithstanding anything to the contrary herein, Cogent expressly disclaims any implied warranty of merchantability or implied warranty of fitness for a particular purpose in connection with the manufacture or use of the Product.

2 OPERATING SPECIFICATIONS

2.1 CSB1726 OPERATING SPECIFICATIONS

The CSB1726 conforms to the following specifications:

Specification	Value
Dimensions	70mm x 50mm x 8mm (no Heatsink on 5.6mm Socket)
Weight	~60g
Storage Temperature	-20C to +100C
Operating Temperature	0C to +70C (requires application specific thermal solution)
Humidity	0% to 95% RH, Non-Condensing
Input Voltage (VIN)	+8V to +14V, Nominal +12V, 2.5A Peak
Output Voltage (VCC3)	+3.3V +/- 10%, 4A Maximum
IPM Voltage (VCC3SB)	3.3V +/- 10%, <100ma Maximum
Power Consumption	12W Typical, 16W Maximum

Table 1 – CSB1726 Operating Specifications

3 OVERVIEW

3.1 INTRODUCTION

The CSB1726 was designed and developed by Cogent Computer Systems, Inc. as a highly integrated Marvell MV78x60 System On a Module (SOM). The CSB1726 provides a small, powerful, flexible engine for embedded control systems of all kinds. The major features of the CSB1726 are as follows:

- **CPU** - 1.333Ghz Quad ARMv6/7 Cores (MV78460), 1Ghz Dual Core Option (MV78260)
- **CACHE** - 32KByte Instruction and Data Caches; 2MByte L2 Cache (1MByte on MV78260)
- **FPU** - IEEE 754 Compliant Single/Double Precision Floating Point Unit
- **SDRAM** - 2GByte 64-Bit Wide DDR3-1066 Memory with 8-Bit ECC
- **FLASH** - On-Board 8MByte SPI NOR and 512MByte SLC NAND
- **PCI EXPRESS** - One x4 and Two x1 Ports
- **1 GIGABIT ETHERNET** - Two 10/100/1000 Auto Select Copper/SGMII/1000-Base-X ports
- **2.5 GIGABIT ETHERNET** - Two 2.5G Capable SGMII Ports
- **SECURITY** - Dual On-Chip Cryptographic and Security Acceleration Engines Support Various Encryption/Decryption Algorithms: AES128; DES/3DES; MD-5 and SHA1 hashing; and others
- **XOR/RAID** - Four High Speed XOR DMA Engines for RAID Storage Applications
- **SATA** - Two SATA Gen 2 (1.5Gbit or 3Gbit/sec) Channel
- **USB** - Two 480Mbit USB 2.0 Host Ports (may also be used as device on carrier)
- **SD/MMC** - 4-Bit SD/MMC Controller (4-Bit SDIO Compliant)
- **SERIAL I/O** - Two 4-wire and One 2-Wire TTL Serial Ports; Two I2C Ports; One SPI Port
- **VIDEO** - On-Chip LCD Controller up to 1024 x 768 via 18-Bit LVDS Output
- **OPERATING VOLTAGE** - 12V Input Rail; On-Board 3.3V (for I/O with 3 Amp available to off board devices), 1.5V (SDRAM) and 1.0V (CPU Core) Power Supplies
- **POWER MANAGEMENT** - On-Board ATXMEGA Microcontroller for Power Sequencing, Boot Configuration, FAN Control and Thermal Monitoring
- **OPERATING TEMPERATURE** - 0C to +70C Standard
- **POWER (DUAL CORE)** - 8W typ., 12W Max and <10mw Power Down
- **POWER (QUAD CORE)** - 12W typ., 16W Max and <10mw Power Down
- **COGENT MXM SOM COMPLIANT** - Common, Interchangeable Footprint across Multiple CPU Architectures (x86, PowerPC, MIPS and ARM); Uses Low Cost Industry Standard MXM-II Socket
- **COMPACT SIZE** - 70mm x 75mm x 8mm (with standard 5.6mm socket, w/o heatsink)

3.2 BLOCK DIAGRAM

Refer to the following figure for a block diagram of the CSB1726 SOM.

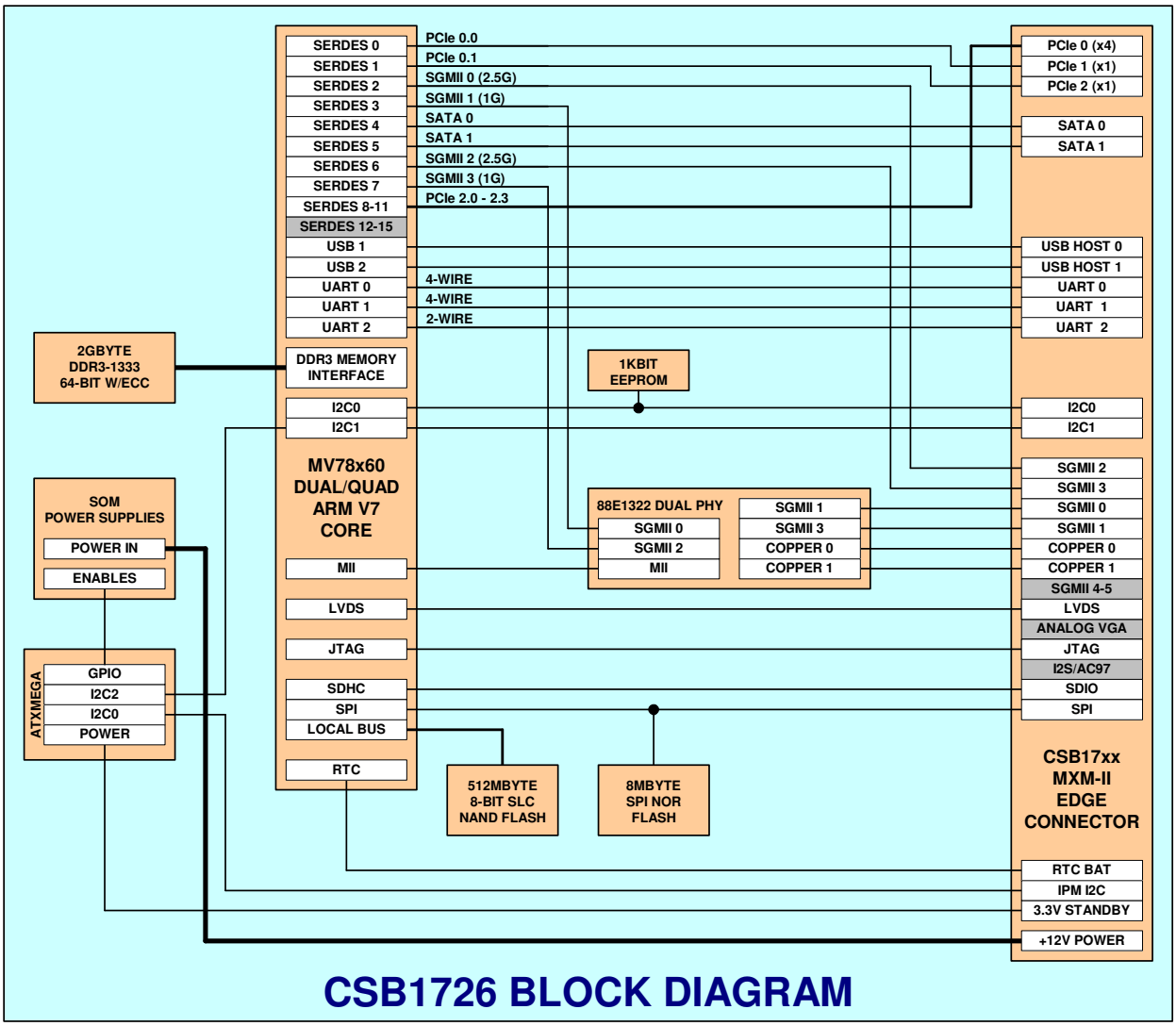

Figure 1 – CSB1726 Block Diagram

4 ON-BOARD DEVICES

4.1 CSB1726 ADDRESS MAP

The following table describes the Address Map of the CSB1726. Refer to the MV78x60 documentation for information regarding on-chip peripheral addressing.

CPU Chip Select	Chip Select Width	Base Address	Size	Description
*DEV_CS0	-	0xF800.0000	-	512MByte NAND
*MCS0	64	0x0000.0000	2GB	2Gbyte DDR3-1066 SDRAM
SPI	-	0xD400.0000	-	M25P64 SPI NOR FLASH
I2C Bus		**I2C Address**		**Description**
I2C0	-	0x50	-	1Kbyte EEPROM

Table 2 – CSB1726 Address Map

4.2 2GBYTE DDR3-1066 SDRAM

The CSB1726 uses nine 256Mx8, DDR3-1066 for a total of 2Gbyte of system memory with Error Checking and Correction (ECC). The MV78x60 memory controller must be programmed for correct operation. Refer to the MV78x60 documentation for more information on programming the SDRAM Memory Controller.

4.3 512MBYTE 8-BIT NAND FLASH

The CSB1726 has a single 8-Bit, 512Mbyte NAND Flash. This device is connected to the MV78x60 device bus. The signals used to interface with the NAND Flash are shown in the following table.

NAND Signal	MV78x60 Signal	Notes
*CE	*DEV_CS0	NAND Chip Select
*WE	*NF_WE	Write Strobe
*RE	*NF_RE	Read Strobe
ALE	DEV_ALE1	Address is latched on the rising edge of *WE when ALE = 1

NAND Signal	MV78x60 Signal	Notes
CLE	DEV_ALE0	Command is latched on the rising edge of *WE when CLE = 1
D0-7	DEV_AD0-DEV_AD7	8-Bit Data bus. Addresses, Commands and Data are transferred via these signals
RDY	DEV_RDY	Device Ready (Busy when 0)

Table 3 – MV78x60 to NAND Flash Connections

4.3.1 NAND FLASH NOTES

1. The Write Protect pin of the NAND Flash is tied high, so no HW Write Protect function is available.
2. At the time this document was written a Micron MT29F4G08ABADAWP, (4Gbit, 512M x 8, SLC) device was populated on the CSB1726. Future versions may ship with the same or larger capacity device. Contact Cogent for updated information on the currently shipping NAND Flash.
3. A Red LED is provided on the CSB1726. This LED is on whenever the NAND RDY signal is low (indicating busy).

4.4 8MBYTE SPI NOR FLASH

The CSB1730 is provided with a Micron M25P64 SPI NOR Flash. This device is connected to the MV78x60 SPI port.

The signals used to interface with the SPI NOR Flash are shown in the following table.

SPI NOR Signal	MV78x60 Signal	Notes
*CE	MPP39/SPI_CS	Chip Select
SO	MPP36/SPI_MOSI	Serial Data to the Flash
SI	MPP37/SPI_MISO	Serial Data from the Flash
SCK	MPP38/SPI_SCK	Clock
*WP	-	Unused, Pulled high
*HOLD	-	Unused, Pulled high

Table 4 – MV78x60 to SPI NOR Flash Connections

4.4.1 SPI NOR FLASH NOTES

1. The SPI NOR Flash is an optional boot device. After boot the SPI Interface should be programmed with optimal timing. Refer to the SPI NOR documentation for more detail.
2. The Write Protect pin of the NAND Flash is tied high, so no HW Write Protect function is available.
3. The HOLD pin is tied high so no hold function is available
4. At the time this document was written a Micron M25P64-VME, (64Mbit, 256 x 8 Page Size, 75Mhz Clock) device was populated on the CSB1726. Future versions may ship with the same or larger capacity device. Contact Cogent for updated information on the currently shipping SPI NOR Flash.

4.5 24AA00T EEPROM

A Microchip 24AA00T EEPROM provides user programmable EEPROM. It is on MV78x60 I2C Bus 0 at I2C address 0x50. The signals used to interface with the 24AA00T are shown in the following table.

24AA00T Signal	MV78x60 Signal	Notes
SCL	TWSI0_SCL	I2C Bus Clock
SDA	TWSI0_SDA	I2C Bus Data

Table 5 – MV78x60 to 24AA00T EEPROM Connections

4.6 MARVELL 88E1322 DUAL PHY

The CSB1726 uses the 88E1322 to interface the two MV78x60 10/100/1000 Gigabit Ethernet Controllers to the system. The 88E1322 supports SGMII to Twisted-Pair Copper or SERDES with auto-detect. The signals used to interface the 88E1322 to the MV78x60 are shown in the following table.

88E1322 Signal	MV78x60 Signal	Notes
P0_S_INN	SRD3_TX_P	SERDES 3 (SGMII 1) Transmit Data Plus
P0_S_INP	SRD3_TX_M	SERDES 3 (SGMII 1) Transmit Data Minus
P0_S_OUTN	SRD3_RX_P	SERDES 3 (SGMII 1) Receive Data Plus

88E1322 Signal	MV78x60 Signal	Notes
P0_S_OUTP	SRD3_RX_M	SERDES 3 (SGMII 1) Receive Data Minus
P2_S_INN	SRD7_TX_P	SERDES 7 (SGMII 3) Transmit Data Plus
P2_S_INP	SRD7_TX_M	SERDES 7 (SGMII 3) Transmit Data Minus
P2_S_OUTN	SRD7_RX_P	SERDES 7 (SGMII 3) Receive Data Plus
P2_S_OUTP	SRD7_RX_M	SERDES 7 (SGMII 3) Receive Data Minus
MDC	MDC	MII Management Bus Clock
MDIO	MDIO	MII Management Bus Data

Table 6 – MV78x60 to 88E1322 Connections

4.6.1 88E1322 INTERFACE NOTES

1. The Copper signals from the 88E1322 are routed to MXM ports GIGE0 and GIGE1. They are designed to connect to a 10/100/1000 compatible transformer (with the transformer center tap connected to GIGE_CTREF and bypassed to ground with a .1uf capacitor). These signals should be routed differentially (100 ohm impedance) and separated from other signals by at least 25mils. The total length from the carrier board MXM Connector to the transformer should be 4” or less.

2. The SERDES signals from the 88E1322 are routed to the CSB17xx SOM ports SGMII 0 and SGMII 1. They are paired with the respective Copper Ports 0 and 1 for auto-detect function.

3. The 88E1322 supports Copper/SGMII or Copper/Fiber Auto-detection. The IPM Micro controls the selection between SGMII and Fiber for the SERDES. Configuration switch %TBD% is used to control this selection at boot time. The default (switch is off or not found) is Fiber.

4. 88E1322 Port 0 and 3 LED outputs LED0, LED1 and LED3 must be programmed for Link 1GBIT, Link 100MBIT and Link any speed respectively. Additionally LED0 should also be programmed to blink during receive or transmit activity.

4.7 ATXMEGA16A4 IPM MICROCONTROLLER

The CSB1726 uses an Atmel ATXMEGA16A4 8-bit Microcontroller to provide configuration, power sequencing and thermal management functions for the MV78x60. The ATXMEGA16A4 is described in more detail in section 7.

5 MV78X60 ON-CHIP PERIPHERALS

5.1 OVERVIEW

The MV78x60 has a number of on-chip peripheral devices as well as a number of user defined Multifunction Programmable Pins (MPP). While it is beyond the scope of this document to provide detailed programming and interfacing information for the MV78x60 on-chip peripherals, the following section describes the assignments for these peripherals and MPP's as they are implemented on the CSB1726.

5.2 MV78X60 TO MXM PERIPHERAL MAPPING

The following table provides a high level view of the mapping from the various MV78x60 peripherals to the MXM ports. Due to pin multiplexing on the MV78x60, not all ports are available.

MV78x60 Peripheral	MXM Port	Description and Notes
TDM	-	Unavailable – pins used by SD/MMC
SPI	SPI	Shared with SPI NOR using SPI_CS1
TWSI0	I2C0	Two-Wire Serial Bus 0
TWSI1	I2C1	Two-Wire Serial Bus 1
LVDS	LVDS	LVDS Display Output
PARALLEL LCD	-	Unavailable, Pins used for GPIO
LCD PWM	LCD_PWM	LCD Brightness Control
UART0	UART0	4-Wire TTL
UART1	UART1	4-Wire TTL
UART2	-	Unavailable, Pins used for UART 0 Handshake
UART3	UART2	2-Wire TTL, TXD/RXD only
USB0	USBH0	480Mbit USB 2.0 Host Port
USB1	USBH1	480Mbit USB 2.0 Host Port
PARALLEL GMII/RGMII	-	Unused – used for GPIO
SERDES 0	PCIe1	PCI Express Port 1, x1

MV78x60 Peripheral	MXM Port	Description and Notes
SERDES 1	PCIe2	PCI Express Port 2, x1
SERDES 2	SGMII 2	SGMII Port 2, 1G/2.5G
SERDES 3	COPPER 0/ SGMII 0	Auto-Detect Copper/SERDES via 88E1322 PHY
SERDES 4	SATA 0	SATA Port 0
SERDES 5	SATA 1	SATA Port 1
SERDES 6	SGMII 3	SGMII Port 3, 1G/2.5G
SERDES 7	COPPER 1/ SGMII 1	Auto-Detect Copper/SERDES via 88E1322 PHY
SERDES 8-11	PCIe 0	PCI Express Port 0, x1 or x4
SERDES 12-15	-	Unused

Table 7 – MV78x60 to MXM Port Mapping

5.3 MV78X60 CHIP SELECTS

As described in Section 4.1, the MV78x60 Chip Selects are used to enable the various devices on the CSB1726.

5.4 MV78X60 MULTI- PURPOSE PIN ASSIGNMENTS

The MV78x60 has 50 Multi- Purpose Pins (0 to 49). The usage on the CSB1726 is described in the following table. It is the responsibility of software to setup these bits for the correct direction and default state as well as the assignment of alternate functions.

MV78x60 MPP	DIR	CSB1726 Usage	Description and Notes
0	IN	*PE0_WAKE	Wakeup from PCIe Port 0
1-3	-	-	Unused
4	IN	*I2C_INT	I2C Devices Shared Interrupt
5	IN	SG3_SD	SGMII Port 3 Signal Detect
6	IN	SG2_SD	SGMII Port 2 Signal Detect
7	IN	SG1_SD	SGMII Port 1 Signal Detect
8	IN	SG0_SD	SGMII Port 0 Signal Detect

MV78x60 MPP	DIR	CSB1726 Usage	Description and Notes
9	IN	PE0_DIR	PCIe Port 0 Direction, 0 = Root, 1 = Endpoint
10-15	-	-	Unused
16	IN	*MII_INT	MII Bus Interrupt from External PHY(s)
17	-	-	Unused
18	I/O	GPIO0	General Purpose I/O
19	I/O	GPIO1	General Purpose I/O
20	IN	*PE1_WAKE	Wakeup from PCIe Port 1
21	IN	PE1_DIR	PCIe Port 1 Direction, 0 = Root, 1 = Endpoint
22	OUT	*SA0_ACT	SATA Port 0 Activity Indicator
23	OUT	*SA1_ACT	SATA Port 1 Activity Indicator
24	-	-	Unused
25	IN	*SD_CD	SD/MMC Card Detect
26	-	-	Unused
27	OUT	LCD_BKL	LCD Backlight Enable
28	OUT	LCD_PWM	LCD Brightness control
29	IN	SD_WP	SD/MMC Write Protect
30	OUT	SD_CLK	SD/MMC Clock
31	I/O	SD_CMD	SD/MMC Command
32-35	I/O	SD_D0-3	SD/MMC Data Bus
36	OUT	SPI_MOSI	SPI Master Out/Slave In
37	IN	SPI_MISO	SPI Master In/Slave Out
38	OUT	SPI_CLK	SPI Clock
39	OUT	*ROM_CS	(*SPI_CS0) M25P64 Chip Select
40	OUT	*SPI_CS	(*SPI_CS1) SPI Port Chip Select
41	-	-	Unused
42	IN	U0_CTS	(UA0_CTS) UART 0 Clear To Send
43	OUT	U0_RTS	(UA0_RTS) UART 0 Request To Send
44	IN	U2_RXD	(UA3_RXD) UART 2 Receive Data

MV78x60 MPP	DIR	CSB1726 Usage	Description and Notes
45	OUT	U2_TXD	(UA3_TXD) UART 2 Transmit Data
46	OUT	U1_RTS	(UA1_RTS) UART 1 Request To Send
47	IN	U1_CTS	(UA1_CTS) UART 1 Clear To Send
48-54	-	-	Unused
55	OUT	CPUA_PD	CPU Core A Power Down to IPM
56	OUT	CPUB_PD	CPU Core B Power Down to IPM
57	OUT	CPUCD_PD	CPU Core C and D Power Down to IPM
58-66	-	-	Unused

Table 8 – MV78x60 MPP Pin Assignments

5.5 MV78X60 UARTS

The MV78x60 has 4 UARTS. Due to pin multiplexing restrictions, UART2 is Unavailable as are UART3 handshaking TXD and RXD are available. UART 0 is routed to the MXM Connector as shown in the following table. Refer to the MV78x60 documentation for more information about the MV78x60 UARTS.

MV78x60 Signal	MXM Signal	Notes
U0_TXD/MPP10	U0_TXD	UART 0 Transmit
U0_RXD/MPP11	U0_RXD	UART 0 Receive

Table 9 – MV78x60 to MXM UART Connections

5.6 MV78X60 I2C INTERFACES

The MV78x60 has two I2C Interfaces. Both are High Speed (100Khz/400Khz), master/slave I2C Serial Controllers. The MV78x60 I2C Controllers are routed to the MXM Connector as shown in the following table. Refer to the MV78x60 documentation for detailed programming information on both I2C controllers.

MV78x60 Signal	MXM Signal	Notes
TW0_SCL/MPP9	I2C0_SCL	I2C Bus 0 Clock
TW0_SDA/MPP8	I2C0_SDA	I2C Bus 0 Data

MV78x60 Signal	MXM Signal	Notes
MPP49	*I2C0_INT	I2C Bus 0 Interrupt
TW1_SCL/MPP37	I2C1_SCL	I2C Bus 1 Clock
TW1_SDA/MPP36	I2C1_SDA	I2C Bus 1 Data

Table 10 – MV78x60 to MXM I2C Connections

5.7 MV78X60 LOCAL BUS INTERFACE

The MV78x60 support a 32-bit Data bus for expansion use. The NAND Flash is connected to this bus on the CSB1726. This bus is not available off board. Refer to the MV78x60 documentation for detailed programming information on the Local Bus Interface.

5.8 MV78X60 HIGH SPEED SERDES PORTS

The MV78460 supports 16 SERDES Ports (12 on MV78260). Each port supports up to 5GB/s bandwidth. The MV78x60 SERDES Ports are routed to the MXM Connector as shown in the following table. Refer to the MV78x60 documentation for detailed programming information on the High Speed SERDES.

SERDES	CSB1726 Usage	Description and Notes
0	PCIe1	PCI Express Port 1, x1
1	PCIe2	PCI Express Port 2, x1
2	SGMII 2	SGMII Port 2, 1G/2.5G
3	COPPER 0/ SGMII 0	Auto-Detect Copper/SERDES via 88E1322 PHY
4	SATA 0	SATA Port 0
5	SATA 1	SATA Port 1
6	SGMII 3	SGMII Port 3, 1G/2.5G
7	COPPER 1/ SGMII 1	Auto-Detect Copper/SERDES via 88E1322 PHY
8-11	PCIe 0	PCI Express Port 0, x1 or x4
12-15	-	Unused

Table 11 – MV78x60 SERDES to MXM Port Mapping

5.8.1 MV78X60 HIGH SPEED SERDES NOTES

1. SERDES 0-2, 4-6 and 8-11 are directly connected to the MXM Connector. As such, some of them may be re-assigned to other available functions as desired by the user. The assignments listed in the table are those defined by Cogent for use with standard Cogent Carrier boards.
2. PCI Express controllers may be defined by software as root ports or endpoints individually. The PCIe_DIR0/1 signals are simply flags from the carrier and do not directly control the interfaces.
3. The optional PCI Express wakeup signals are GPIO mode inputs and must be enabled by software.

5.9 MV78X60 USB CONTROLLER

The MV78x60 has three 480Mbit, USB 2.0 Ports. USB Ports 0 and 1 are routed to the MXM Connector and may be used as host or device. USB Port 2 is unused. Refer to the MV78x60 documentation for detailed programming information on the USB Controllers.

5.10 MV78X60 LCD CONTROLLER

The MV78x60 contains an LCD interface that supports both 24-Bit Parallel LCD and 24-Bit LVDS outputs. On the CSB1726 the LVDS interface (18-Bit only) goes to the MXM Connector LVDS Port, while the parallel interface signals are used for other functions.

6 CSB1726 CLOCKING

6.1 MV78X60 INPUT CLOCKS

The MV78x60 is provided with several input clocks as described in the following table.

CLOCK	Description and Notes
REF_CLK_XIN	25Mhz clock. Used by the MV78x60 to create its core clock, as well as the DDR clock, SERDES, Platform and Local Bus clocks.
RTC_XIN/XOUT	32.768Khz clock. MV78x60 Real Time Clock.
PEX0_CLK	100Mhz differential clock from MXM Connector REF_CLK. Used as reference clock for all MV78x60 SERDES defined as PCI Express.

Table 12 – MV78x60 Input Clocks

6.2 MV78X60 OUTPUT CLOCKS

The MV78x60 drives several output clocks as described in the following table. Note that the output frequency of M_CLK is defined during configuration. The rest must be defined by software, equal to or less than the listed maximum frequency.

CLOCK	Description and Notes
M_CLK	Differential Memory Clock, 667Mhz
SD_CLK	SD/MMC up to 50Mhz
LVDS_CLK	LVDS Display Clock up to 700Mhz (100Mhz Pixel Clock)
I2C0_SCL	I2C Bus 1 Clock up to 400Khz
I2C1_SCL	I2C Bus 2 Clock up to 400Khz

Table 13 – MV78x60 Output Clocks

6.3 88E1322 CLOCK

The 88E1121R is supplied with a 25Mhz reference clock.

7 CSB1726 POWER MANAGEMENT

7.1 OVERVIEW

The CSB1726 has a sophisticated power management mechanism using an Atmel ATXMEGA16A4 8-bit Microcontroller.

7.2 ATXMEGA16A4 IPM MICROCONTROLLER

The ATXMEGA16A4 8-bit Microcontroller is used to provide the following features: power supply sequencing; MV78x60 configuration; clock PLL programming; MV78x60 power sequencing; and off-board power supply control. The ATXMEGA16A4 uses a number of internal peripherals and GPIO's to perform these tasks. The following table lists the ATXMEGA16A4 signals and peripherals used on the CSB1726.

XMEGA 16A4 Port	DIR	CSB1726 Usage	Description and Notes
PA0	IN	VOK_IO	I/O Rail Regulators Power Good
PA1	IN	VOK_AB	MV78x60 CPU A and B Voltage Regulator Power Good
PA2	IN	VOK_CD	MV78x60 CPU C and D Voltage Regulator Power Good
PA3	IN	VOK_SOC	MV78x60 Platform Voltage Regulator Power Good
PA4	IN	*RST_IN	MXM Reset In
PA5	IN	*RST_OUT	Reset Output from MV78x60
PA6	-	-	Unused
PA7	OUT	*TRST	JTAG Reset to MV78x60 (or'ed with reset from the MXM JTAG port)
PB0	IN	CPUB_PD	CPU B Power Down Request
PB1	IN	CPUA_PD	CPU A Power Down Request
PB2	IN	CPUCD_PD	CPU C and D Power Down Request
PB3	OUT	*LOW_PWR	Low Power Flag to system
PC0	I/O	IPM_SDA	IPM I2C Bus Data to/from MXM. Used to control target power supply and read configuration Switches
PC1	I/O	IPM_SCL	IPM I2C Clock to/from MXM. Used to control target power supply and read configuration Switches

XMEGA 16A4 Port	DIR	CSB1726 Usage	Description and Notes
PC2	I/O	*IPM_INT	IPM I2C Bus Interrupt/Alert. Currently unused.
PC3	-	-	Unused
PC4	OUT	FAN	Fan Control signal to target board
PC5	IN	TACH	Fan Tachometer from Target Board
PC6	-	-	Unused
PC7	OUT	*CRST	MV78x60 CPU Reset
PD0	OUT	ETH_SEL	Set 88E1322 PHY SERDES to SGMII (1) or Fiber (0)
PD1	-	-	Unused
PD2	-	-	Unused
PD3	PUT	VEN_SOC	MV78x60 Platform Voltage Regulator Enable
PD4	OUT	*VEN_AB	MV78x60 CPU A and B Voltage Regulator Enable
PD5	OUT	*VEN_CD	MV78x60 CPU C and D Voltage Regulator Enable
PD6	OUT	*V33_EN	3.3V Regulator Enable
PD7	OUT	*V15_EN	1.5V Regulator Enable
PE0	I/O	I2C0_SDA	I2C Data to Configuration Expanders
PE1	I/O	I2C0_SCL	I2C Data to Configuration Expanders
PE2	-	-	Unused
PE3	-	-	Unused
PR0	-	-	Unused
PR1	-	-	Unused

Table 14 – ATXMEGA16A4 Peripheral and GPIO usage

7.2.1 ATXMEGA16A4 MICROCONTROLLER NOTES

1. All information regarding the pinout, usage and presence of the ATXMEGA16A4 is subject to change and is provided for informational purposes only.
2. Future versions of the CSB1726 may use other versions of the ATXMEGA family or even different IPM Microcontrollers altogether.
3. The ATXMEGA16A4 provides configuration strapping to the MV78x60 via

two on-board I2C registers. The MV78x60 configuration process is described in detail in section 8.

7.3 IPM CONFIGURATION INTERFACE

The ATXMEGA16A4 software probes for the presence of a PCA9554 located on the IPM I2C Bus at address 0x27. It is used to read an 8-bit value to determine the proper configuration of the CSB1726. This can be a switch, header with jumpers, or hard-wired on the target board. The bit assignments for the CSB1726 are shown in the following table.

PCA9554 Bit	Name	Description and Notes
0	%TBD%	Usage to be determined
1	%TBD%	Usage to be determined
2	%TBD%	Usage to be determined
3	%TBD%	Usage to be determined
4	%TBD%	Usage to be determined
5	%TBD%	Usage to be determined
6	%TBD%	Usage to be determined
7	%TBD%	Usage to be determined

Table 15 – IPM Configuration Interface Bit Assignments

7.3.1 IPM CONFIGURATION INTERFACE NOTES

1. If the probe fails, the ATXMEGA16A4 assumes all values are 1.
2. The ATXMEGA16A4 reads this value whenever it resets the MV78x60, not just at power up.

7.4 IPM POWER SUPPLY INTERFACE

The ATXMEGA16A4 software probes for a PCA9536 located on the IPM I2C Bus at address 0x41. This 4-bit expander is used to interface the CSB1726 with an ATX style power supply. The bit assignments are shown in the following table.

PCS9536 Bit	Name	Description and Notes
0	*PWR_SW	Low True Power On/Off Switch

PCS9536 Bit	Name	Description and Notes
1	*PS_ON	Low True Power On to Power Supply
2	PS_OK	High True Power OK from Power Supply
3	IPM_LED	Low True LED Enable for IPM Use

Table 16 – IPM Power Supply Interface Bit Assignments

7.4.1 IPM POWER SUPPLY INTERFACE NOTES

1. If the probe fails, the ATXMEGA16A4 operates in “Always On Mode 0”. The ATXMEGA16A4 will power up the CSB1726 as soon as VIN reaches the minimum to operate.
2. The ATXMEGA16A4 software monitors the *PWR_SW signal after power up. If it is always low, the ATXMEGA16A4 operates in “Always On Mode 1”. It will sequence the target power supply, then power up the CSB1726.
3. If the PCA9536 is present, the ATXMEGA16A4 will enable the IPM_LED at its own reset. The IPM_LED stays on until the ATXMEGA16A4 has completed powering up the CSB1726, thus providing an indication of successful power up.

8 MV78X60 CONFIGURATION

8.1 OVERVIEW

When it's *SYSRST input is released, the MV78x60 samples a number of pins to set various configuration options. These options and the pins used are detailed in the following table. Refer to the MV78x60 documentation for more information on the overall configuration options.

8.2 DEFAULT CONFIGURATION

The following table lists the configuration pins and the values driven on the CSB1726. Only signals that are driven by the ATXMEGA16A4 are shown. Note that not all values are valid.

MV78x60 PIN	Name	Description and Notes
DEV_AD7	PEX_CLK	0, PCIe reference clock is input
MPP50, DEV_AD15	BOOT_WIDTH	0, NAND Boot Width = 8, SPI Boot Width = 32
DEV_AD[14:11]	BOOT_DEV	0x1 = Boot from NAND Flash **0x3 = Boot from SPI flash** 0x4 = Boot from PCI Express port 0 0x5 = Boot from SATA 0x7 = Internal Boot Rom via UART 0 (UA0)
MPP[2:1]	NAND_SERDES	When Boot from NAND: 0x0 = 512B Page Size **0x1 = 2KB Page Size** 0x2 = 4KB Page Size 0x3 = 8KB Page Size When Boot from SATA: **0x1 = Boot from SERDES 4 (SATA 0)** 0x2 = Boot from SERDES 5 (SATA1)
MPP[13:12]	NAND_ECC	**0x0 = 4-Bit ECC** 0x1 = 8-Bit ECC 0x2 = 12-Bit ECC 0x3 = 16-Bit ECC

MV78x60 PIN	Name	Description and Notes
DEVC_ALE0, DEV_AD[10:8]	CPU0_FREQ	0x0 = 1000Mhz 0x1 = 1066Mhz 0x2 = 1200Mhz **0x3 = 1333Mhz** 0x4 = 1500Mhz 0x9 = 667Mhz 0xA = 800Mhz 0xB = 1600Mhz
DEV_AD[6:3]	SOC_DIV	0x2 = NBCLK = 1:1, HCLK = 1:3, MCLK = 1:1.5 0x5 = NBCLK = 1:2, HCLK = 1:4, MCLK = 1:2 0x9 = NBCLK = 1:2, HCLK = 1:4, MCLK = 1:3 **0xA = NBCLK = 1:2, HCLK = 1:5, MCLK = 1:2.5** 0x9 = NBCLK = 1:2, HCLK = 1:4, MCLK = 1:3 0x13 = NBCLK = 1:1, HCLK = 1:2, MCLK = 1:1 0x14 = NBCLK = 1:1.5, HCLK = 1:3, MCLK = 1:1.5

Table 17 – MV78x60 Configuration Settings

9 CSB1726 SOFTWARE

9.1 OVERVIEW

Due to the various resources contained on the CSB1726, both internal and external to the MV78x60, it is necessary to initialize a large number of MV78x60 registers and external devices before correct operation can begin. These values and their proper sequencing are beyond the scope of this document. Contact Cogent for example boot initialization code.

10 MXM FORMAT/PINOUT

10.1 OVERVIEW

This section provides an introduction to the Cogent MXM form factor as well as the pinout of the MXM edge connector on the CSB1726.

10.2 MXM FORMAT

The CSB1726 is fully compatible with the Cogent CSB17xx family of Cogent MXM SOM (System On a Module) boards. Although this form factor uses the low cost, high performance MXM II connector developed originally for laptop computer graphics cards, the Cogent MXM SOM form factor, pinout and pin orientation are not related to, nor compatible with, any other form factor. The layout of the CSB1726 is shown in the following figures (for illustrative purposes only).

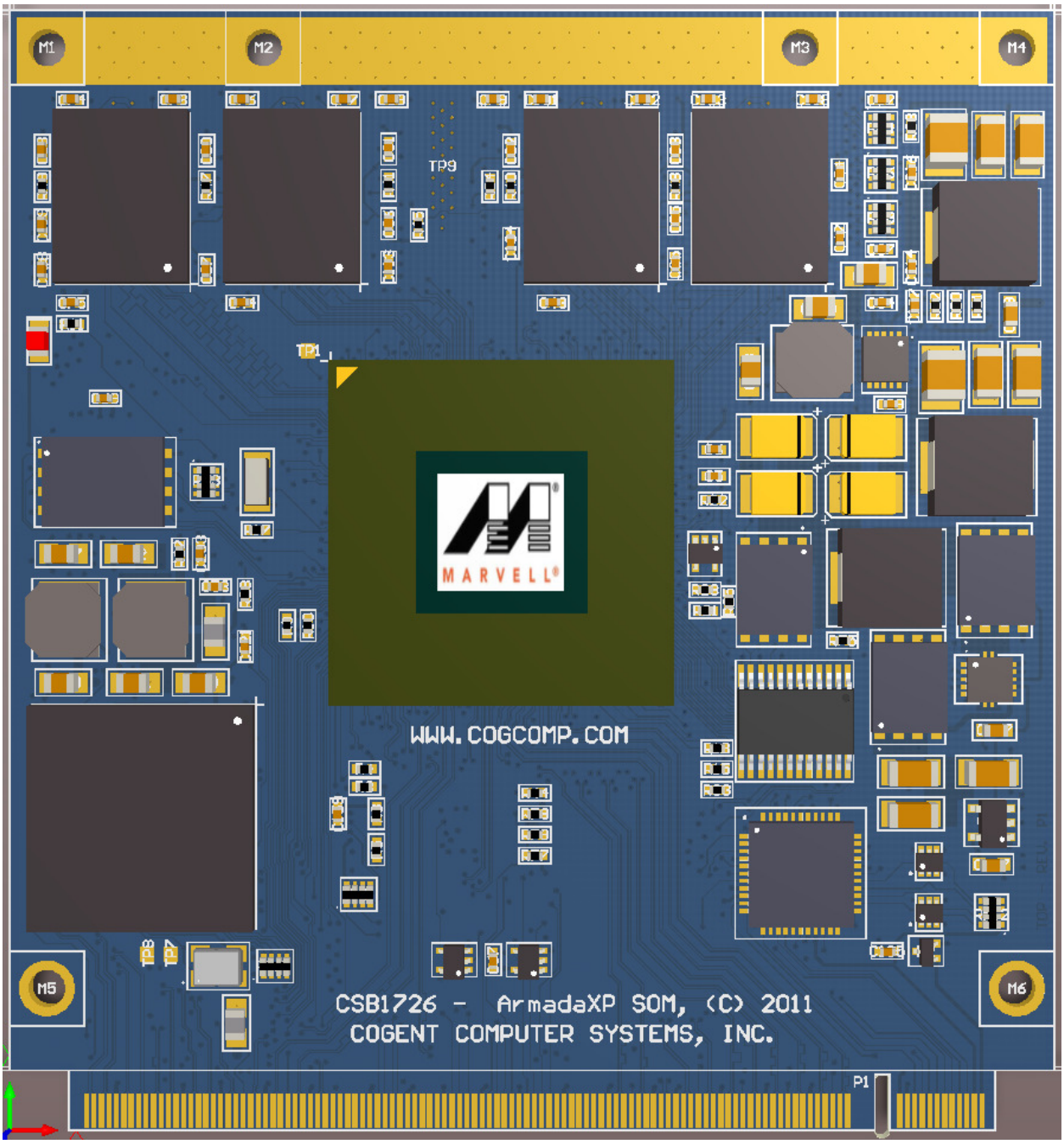

Figure 2 – CSB1726 Top Side Placement

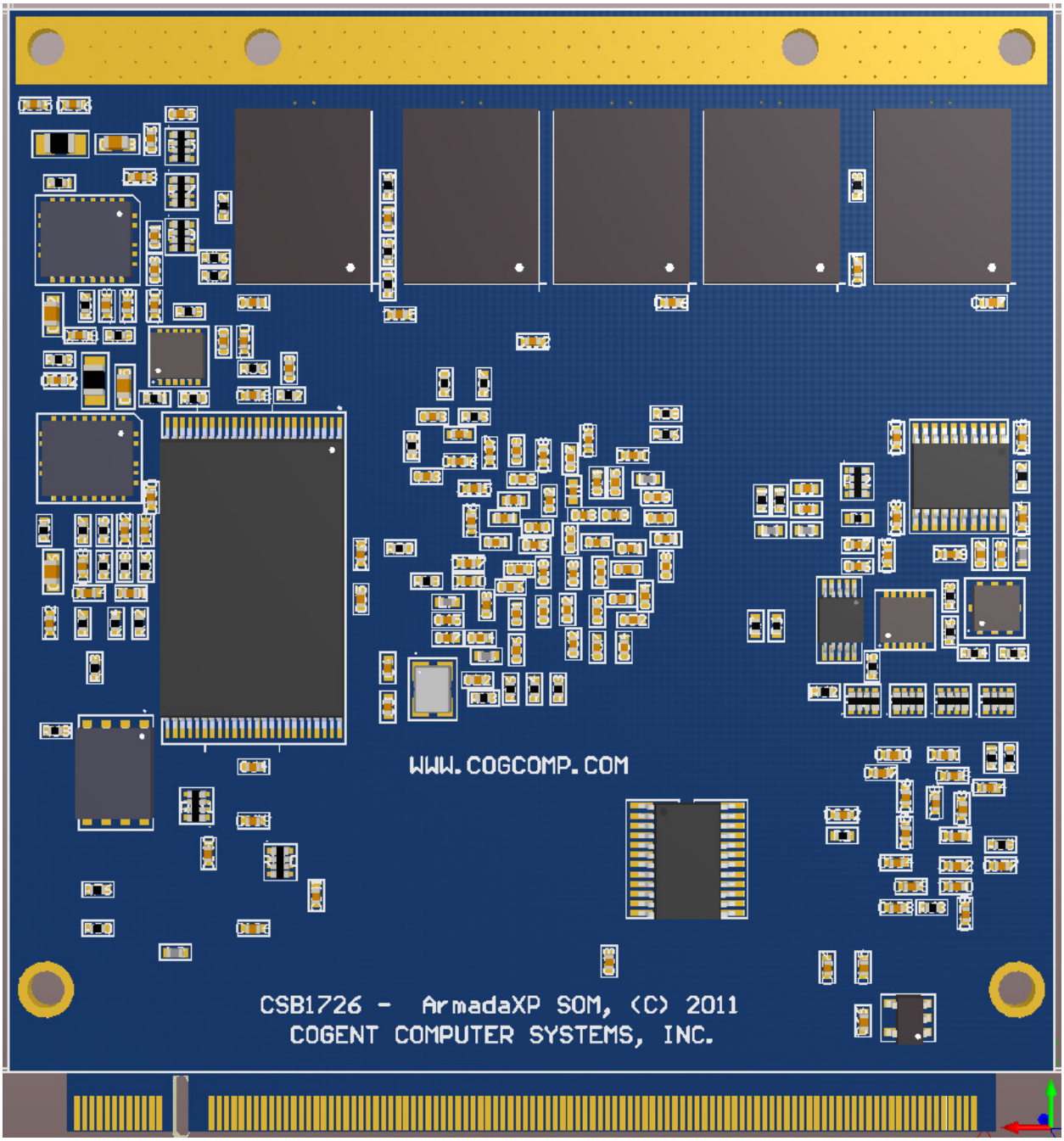

Figure 3 – CSB1726 Bottom Side Placement

10.3 MXM CONNECTOR

The MXM format is an edge card with two sides, A and B. Each side has 115 contacts for a total of 230-pins. The MXM connector is available from multiple vendors and with differing stack heights. Vendor part numbers for this are shown in the following table.

Vendor	Part Number	Mated Height
Foxconn	AS0B326-S78N-7F	5mm
Foxconn	AS0B326-S55N-7F	2.7mm
Foxconn	AS0B326-S43N-7F	1.5mm
Genesis Technology	GTI08-30375	5mm
ACES	88882-2Dxx	5mm
ACES	88885-2Dxx	2.7mm

Table 18 – CSB1726 Connector to Mated Height

10.3.1 MXM CONNECTOR NOTES

1. The mated height refers to the spacing between the bottom side of the CSB1726 PCB and the top surface of the carrier board.
2. The maximum height of any component on the bottom side of the CSB1726 is 1.5mm.

10.4 MXM CONNECTOR PINOUTS

The CSB1726 uses 230 edge fingers to mate with a standard MXM-II socket. The following tables describe the pinout of these connectors. An "N" in the column marked CSB indicates that the signal is not supported by the CSB1726. Power signals are shown in bold. This pinout conforms to the "Network" variant of the Cogent MXM SOM standard.

NOTE: Some of these signals are used during the initial configuration process. As such they must not be driven during the time that *RST_OUT is active (low true). It is the responsibility of the target board designer to insure that any connection to these signals is tri-stated or made input during this time. As a general rule for future compatibility, the target board should disable all signals driven to the SOM when *RST_OUT = 0.

MXM CONNECTOR			
PIN	**NAME**	**CSB**	**CSB1726 USAGE AND NOTES**
A1	**GE0_MDI_0_M**		GIGE 0 MDI 0 MINUS
B1	***GE1_SPD1G**		GIGE 1 SPEED 1GBIT LED
A2	**GE0_MDI_0_P**		GIGE 0 MDI 0 PLUS
B2	***GE0_SPD1G**		GIGE 0 SPEED 1GBIT LED
A3	**GE0_MDI_1_M**		GIGE 0 MDI 1 MINUS

MXM CONNECTOR			
PIN	**NAME**	**CSB**	**CSB1726 USAGE AND NOTES**
B3	***GE1_LNK**		GIGE 1 LINK/ACTIVITY
A4	**GE0_MDI_1_P**		GIGE 0 MDI 1 PLUS
B4	***GE0_LNK**		GIGE 0 LINK/ACTIVITY
A5	**VCC3**		**3.3V OUTPUT**
B5	**VCC3**		**3.3V OUTPUT**
A6	**GE0_MDI_2_M**		GIGE 0 MDI 2 MINUS
B6	***GE1_SPD100**		GIGE 1 SPEED 100MBIT LED
A7	**GE0_MDI_2_P**		GIGE 0 MDI 2 PLUS
B7	***GE0_SPD100**		GIGE 0 SPEED 100MBIT LED
A8	**GE0_MDI_3_M**		GIGE 0 MDI 3 MINUS
B8	**MDIO**		MII BUS DATA FOR EXTERNAL PHYS
A9	**GE0_MDI_3_P**		GIGE 0 MDI 3 PLUS
B9	**MDC**		MII BUS CLOCK FOR EXTERNAL PHYS
A10	**GE1_MDI_3_M**		GIGE 1 MDI 3 MINUS
B10	***MII_INT**		MII BUS INTERRUPT FROM EXTERNAL PHYS
A11	**GE1_MDI_3_P**		GIGE 1 MDI 3 PLUS
B11	***I2C0_INT**		PRIMARY I2C BUS INTERRUPT
A12	**GE1_MDI_2_M**		GIGE 1 MDI 2 MINUS
B12	**I2C0_SCL**		PRIMARY I2C BUS CLOCK
A13	**GE1_MDI_2_P**		GIGE 1 MDI 2 PLUS
B13	**I2C0_SDA**		PRIMARY I2C BUS DATA
A14	**GND**		**GROUND**
B14	**GND**		**GROUND**
A15	**GE1_MDI_1_M**		GIGE 1 MDI 1 MINUS
B15	**GE0_CTREF**		GIGE CENTER TAP REFERENCE VOLTAGE
A16	**GE1_MDI_1_P**		GIGE 1 MDI 1 PLUS
B16	**GE_CTREF**		ALWAYS CONNECT TO B15

MXM CONNECTOR			
PIN	**NAME**	**CSB**	**CSB1726 USAGE AND NOTES**
A17	**GE1_MDI_0_M**		GIGE 1 MDI 0 MINUS
B17	**I2C1_SCL**		SECONDARY I2C BUS CLOCK
A18	**GE1_MDI_0_P**		GIGE 1 MDI 0 PLUS
B18	**I2C1_SDA**		SECONDARY I2C BUS DATA
A19	**VCC3**		**3.3V OUTPUT**
B19	**VCC3**		**3.3V OUTPUT**
A20	**SG1_TD_M**		SGMII 1 TRANSMIT MINUS
B20	**SG1_RD_M**		SGMII 1 RECEIVE MINUS
A21	**SG1_TD_P**		SGMII 1 TRANSMIT PLUS
B21	**SG1_RD_P**		SGMII 1 RECEIVE PLUS
A22	**SG1_SD**		SGMII 1 SIGNAL DETECT
B22	**SG0_SD**		SGMII 0 SIGNAL DETECT
A23	**SG0_TD_M**		SGMII 0 TRANSMIT MINUS
B23	**SG0_RD_M**		SGMII 0 RECEIVE MINUS
A24	**SG0_TD_P**		SGMII 0 TRANSMIT PLUS
B24	**SG0_RD_P**		SGMII 0 RECEIVE PLUS
A25	**GND**		**GROUND**
B25	**GND**		**GROUND**
A26	**SA1_TD_M**		CPU SATA 1 TRANSMIT MINUS
B26	**SA1_RD_M**		CPU SATA 1 RECEIVE MINUS
A27	**SA1_TD_P**		CPU SATA 1 TRANSMIT PLUS
B27	**SA1_RD_P**		CPU SATA 1 RECEIVE PLUS
A28	***SA1_ACT**		SATA 1 ACTIVITY
B28	***SA0_ACT**		SATA 0 ACTIVITY
A29	**SA0_TD_M**		CPU SATA 0 TRANSMIT MINUS
B29	**SA0_RD_M**		CPU SATA 0 RECEIVE MINUS
A30	**SA0_TD_P**		CPU SATA 0 TRANSMIT PLUS

MXM CONNECTOR			
PIN	**NAME**	**CSB**	**CSB1726 USAGE AND NOTES**
B30	**SA0_RD_P**		CPU SATA 0 RECEIVE PLUS
A31	**VCC3**		**3.3V OUTPUT**
B31	**VCC3**		**3.3V OUTPUT**
A32	**UH1_M**		USB HOST PORT 1 MINUS
B32	**UH0_M**		USB HOST PORT 0 MINUS
A33	**UH1_P**		USB HOST PORT 1 PLUS
B33	**UH0_P**		USB HOST PORT 0 PLUS
A34	**GND**		**GROUND**
B34	**GND**		**GROUND**
A35	**VGA_R**	N	ANALOG VGA RED
B35	**VGA_HS**	N	ANALOG VGA HORIZONTAL SYNC
A36	**VGA_G**	N	ANALOG VGA GREEN
B36	**VGA_VS**	N	ANALOG VGA VERTICAL SYNC
A37	**VGA_B**	N	ANALOG VGA BLUE
B37	**I2S_MCLK**	N	I2S MASTER CLOCK
A38	**TDM_RFS/ *TDM_INT**	N	TDM RECEIVE FRAME SYNC OR TDM INTERRUPT
B38	**TDM_RCK/ *TDM_RST**	N	TDM RECEIVE CLOCK OR TDM RESET
A39	**VCC3**		**3.3V OUTPUT**
B39	**VCC3**		**3.3V OUTPUT**
A40	**MC_CLK**		SD/MMC CLOCK
B40	**MC_CS_D3**		SD/MMC DATA 3 (SPI CS)
A41	**MC_DIN_CMD**		SD/MMC COMMAND (SPI MOSI)
B41	**MC_DOUT_D0**		SD/MMC DATA 0 (SPI MISO)
A42	**MC_IRQ_D1**		SD/MMC DATA 1 (SPI/SDIO IRQ)
B42	**MC_D2**		SD/MMC DATA 2

MXM CONNECTOR			
PIN	**NAME**	**CSB**	**CSB1726 USAGE AND NOTES**
A43	**MC_WP**		SD/MMC WRITE PROTECT
B43	***MC_CD**		SD/MMC DETECT
A44	**GND**		**GROUND**
B44	**GND**		**GROUND**
A45	**I2S_BCLK**	N	I2S BIT CLOCK
B45	**I2S_LRCLK**	N	I2S LEFT/RIGHT CLOCK
A46	**I2S_TXD**	N	I2S TRANSMIT DATA
B46	**I2S_RXD**	N	I2S RECEIVE DATA
A47	**SSI_CLK/ TDM_CLK**	N	SSI CLOCK OR TDM CLOCK
B47	**SSI_SYNC/ TDM_FS**	N	SSI FRAME SYNEC OR TDM FRAME SYNC
A48	**SSI_TXD/ TDM_TXD**	N	SSI TRANSMIT DATA OR TDM TRANSMIT DATA
B48	**SSI_RXD/ TDM_RXD**	N	SSI RECEIVE DATA OR TDM RECEIVE DATA
A49	**VCC3**		**3.3V OUTPUT**
B49	**VCC3**		**3.3V OUTPUT**
A50	**SPI_CLK**		SPI CLOCK
B50	***SPI_CS**		SPI CHIP SELECT
A51	**SPI_MOSI**		SPI MASTER OUT
B51	**SPI_MISO**		SPI MASTER IN
A52	**U2_TXD**		UART 2 TRANSMIT
B52	**U2_RXD**		UART 2 RECEIVE
A53	**U2_RTS**	N	UART 2 CLEAR TO SEND
B53	**U2_CTS**	N	UART 2 REQUEST TO SEND
A54	**GND**		**GROUND**
B54	**GND**		**GROUND**

MXM CONNECTOR			
PIN	**NAME**	**CSB**	**CSB1726 USAGE AND NOTES**
A55	**U1_TXD**		UART 1 TRANSMIT
B55	**U1_RXD**		UART 1 RECEIVE
A56	**U1_RTS**		UART 1 CLEAR TO SEND
B56	**U1_CTS**		UART 1 REQUEST TO SEND
A57	**U0_TXD**		UART 0 TRANSMIT
B57	**U0_RXD**		UART 0 RECEIVE
A58	**U0_RTS**		UART 0 CLEAR TO SEND
B58	**U0_CTS**		UART 0 REQUEST TO SEND
A59	**VCC3**		**3.3V OUTPUT**
B59	**VCC3**		**3.3V OUTPUT**
A60	***RST_IN**		SOM RESET IN
B60	***RST_OUT**		SOM RESET OUT
A61	***TRST**		JTAG RESET
B61	**TCK**		JTAG CLOCK
A62	**TMS**		JTAG MODE
B62	**TDI**		JTAG DATA IN
A63	**TDO**		JTAG DATA OUT
B63	**DBG0**		DEBUG SIGNAL 0 - JTAG MODE SOC (TMS_SOC)
A64	**DBG1**	N	DEBUG SIGNAL 1
B64	**DBG2**	N	DEBUG SIGNAL 2
A65	**GND**		**GROUND**
B65	**GND**		**GROUND**
A66	**SD3_TD_M**		CPU SERDES 3 TRANSMIT MINUS
B66	**SD3_RD_M**		CPU SERDES 3 RECEIVE MINUS
A67	**SD3_TD_P**		CPU SERDES 3 TRANSMIT PLUS
B67	**SD3_RD_P**		CPU SERDES 3 RECEIVE PLUS
A68	**SD3_IO**		CPU SERDES 3 I/O

MXM CONNECTOR			
PIN	**NAME**	**CSB**	**CSB1726 USAGE AND NOTES**
B68	**SD2_IO**	N	CPU SERDES 2 I/O
A69	**SD2_TD_M**	N	CPU SERDES 2 TRANSMIT MINUS
B69	**SD2_RD_M**	N	CPU SERDES 2 RECEIVE MINUS
A70	**SD2_TD_P**	N	CPU SERDES 2 TRANSMIT PLUS
B70	**SD2_RD_P**	N	CPU SERDES 2 RECEIVE PLUS
A71	**VCC3**		**3.3V OUTPUT**
B71	**VCC3**		**3.3V OUTPUT**
A72	**SD1_TD_M**		SGMII 3 TRANSMIT MINUS
B72	**SD1_RD_M**		SGMII 3 RECEIVE MINUS
A73	**SD1_TD_P**		SGMII 3 TRANSMIT PLUS
B73	**SD1_RD_P**		SGMII 3 RECEIVE PLUS
A74	**SD1_IO**		SGMII 3 SIGNAL DETECT
B74	**SD0_IO**		SGMII 2 SIGNAL DETECT
A75	**SD0_TD_M**		SGMII 2 TRANSMIT MINUS
B75	**SD0_RD_M**		SGMII 2 RECEIVE MINUS
A76	**SD0_TD_P**		SGMII 2 TRANSMIT PLUS
B76	**SD0_RD_P**		SGMII 2 RECEIVE PLUS
A77	**GND**		**GROUND**
B77	**GND**		**GROUND**
A78	**REF_CLK_M**		PCI EXPRESS REFERENCE CLOCK MINUS
B78	**SD_CLK_M**	N	CPU SERDES REFERENCE CLOCK MINUS
A79	**REF_CLK_P**		PCI EXPRESS REFERENCE CLOCK PLUS
B79	**SD_CLK_P**	N	CPU SERDES REFERENCE CLOCK MINUS
A80	**VCC3**		**3.3V OUTPUT**
B80	**VCC3**		**3.3V OUTPUT**
A81	**LV_CK_M**		LVDS CLOCK MINUS
B81	**LV_D2_M**		LVDS DATA 2 MINUS

MXM CONNECTOR			
PIN	**NAME**	**CSB**	**CSB1726 USAGE AND NOTES**
A82	**LV_CK_P**		LVDS CLOCK PLUS
B82	**LV_D2_P**		LVDS DATA 2 PLUS
A83	**LCD_PWM**		LCD BRIGHTNESS PWM CONTROL
B83	**LCD_BKL**		LCD BACKLIGHT POWER ENABLE
A84	**LV_D1_M**		LVDS DATA 1 MINUS
B84	**LV_D0_M**		LVDS DATA 0 MINUS
A85	**LV_D1_P**		LVDS DATA 1 PLUS
B85	**LV_D0_P**		LVDS DATA 0 PLUS
A86	**GND**		**GROUND**
B86	**GND**		**GROUND**
A87	**PE2_TD_M**		PCI EXPRESS LINK 2, TRANSMIT MINUS
B87	**PE2_RD_M**		PCI EXPRESS LINK 2, RECEIVE MINUS
A88	**PE2_TD_P**		PCI EXPRESS LINK 2, TRANSMIT PLUS
B88	**PE2_RD_P**		PCI EXPRESS LINK 2, RECEIVE PLUS
A89	**PE1_DIR**		PCI EXPRESS LINK 1 DIRECTION
B89	***PE1_WAKE**		PCI EXPRESS LINK 1 WAKEUP
A90	**PE1_TD_M**		PCI EXPRESS LINK 1, TRANSMIT MINUS
B90	**PE1_RD_M**		PCI EXPRESS LINK 1, RECEIVE MINUS
A91	**PE1_TD_P**		PCI EXPRESS LINK 1, TRANSMIT PLUS
B91	**PE1_RD_P**		PCI EXPRESS LINK 1, RECEIVE PLUS
A92	**VCC3**		**3.3V OUTPUT**
B92	**VCC3**		**3.3V OUTPUT**
A93	**PE0_TD3_M**		PCI EXPRESS LINK 0, LANE 3 TRANSMIT MINUS
B93	**PE0_RD3_M**		PCI EXPRESS LINK 0, LANE 3 RECEIVE MINUS
A94	**PE0_TD3_P**		PCI EXPRESS LINK 0, LANE 3 TRANSMIT PLUS
B94	**PE0_RD3_P**		PCI EXPRESS LINK 0, LANE 3 RECEIVE PLUS
A95	**RSVD**	N	RESERVED

MXM CONNECTOR			
PIN	**NAME**	**CSB**	**CSB1726 USAGE AND NOTES**
B95	**RSVD**	N	RESERVED
A96	**PE0_TD2_M**		PCI EXPRESS LINK 0, LANE 2 TRANSMIT MINUS
B96	**PE0_RD2_M**		PCI EXPRESS LINK 0, LANE 2 RECEIVE MINUS
A97	**PE0_TD2_P**		PCI EXPRESS LINK 0, LANE 2 TRANSMIT PLUS
B97	**PE0_RD2_P**		PCI EXPRESS LINK 0, LANE 2 RECEIVE PLUS
A98	**GND**		**GROUND**
B98	**GND**		**GROUND**
A99	**PE0_TD1_M**		PCI EXPRESS LINK 0, LANE 1 TRANSMIT MINUS
B99	**PE0_RD1_M**		PCI EXPRESS LINK 0, LANE 1 RECEIVE MINUS
A100	**PE0_TD1_P**		PCI EXPRESS LINK 0, LANE 1 TRANSMIT PLUS
B100	**PE0_RD1_P**		PCI EXPRESS LINK 0, LANE 1 RECEIVE PLUS
A101	**PE0_DIR**		PCI EXPRESS LINK 0 DIRECTION
B101	***PE0_WAKE**		PCI EXPRESS LINK 0 WAKEUP
A102	**PE0_TD0_M**		PCI EXPRESS LINK 0, LANE 0 TRANSMIT MINUS
B102	**PE0_RD0_M**		PCI EXPRESS LINK 0, LANE 0 RECEIVE MINUS
A103	**PE0_TD0_P**		PCI EXPRESS LINK 0, LANE 0 TRANSMIT PLUS
B103	**PE0_RD0_P**		PCI EXPRESS LINK 0, LANE 0 RECEIVE PLUS
A104	**GND**		**GROUND**
B104	**GND**		**GROUND**
A105	**VCC3**		**3.3V OUTPUT**
B105	**VCC3**		**3.3V OUTPUT**
A106	**IPM_SCL**		IPM MICRO I2C BUS CLOCK
B106	**VIN**		SOM POWER IN
A107	**IPM_SDA**		IPM MICRO I2C BUS DATA
B107	**VIN**		SOM POWER IN
A108	***IPM_INT**		IPM MICRO INTERRUPT
B108	**VIN**		SOM POWER IN

MXM CONNECTOR			
PIN	**NAME**	**CSB**	**CSB1726 USAGE AND NOTES**
A109	***IPM_RST**		IPM MICRO RESET
B109	**VIN**		SOM POWER IN
A110	**IPM_DBG**		IPM MICRO DEBUG
B110	**VIN**		SOM POWER IN
A111	**IPM_RFU**		RESERVED FOR FUTURE IPM USE
B111	**VIN**		SOM POWER IN
A112	**FAN**		CPU FAN CONTROL
B112	**VIN**		SOM POWER IN
A113	**TACH**		CPU FAN SPEED
B113	**VIN**		SOM POWER IN
A114	**VCC3_SB**		POWER TO IPM DEVICES
B114	**VIN**		SOM POWER IN
A115	**RTC_BAT**		RTC BATTERY BACKUP POWER
B115	**VIN**		SOM POWER IN

Table 19 – CSB1726 MXM Connector Pinout

11 DOCUMENT REVISIONS

Date	Revision	Change
8/29/2011	P1.0	First Release

Table 20 – Document Revisions